Notice of Allowability	Application No. 09/418,706	Applicant(s) ABTS ET AL.	
	Examiner Samuel Broda	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Response mailed on 20 May 2004*.

2. ☒ The allowed claim(s) is/are *2-19, 21-32, and 34-43*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☒ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☒ to Paper No./Mail Date *3*.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER

1. This communication is in response to Applicants' Response to Notice of Non-Responsive Amendment mailed on 20 May 2004. Claims 2, 5-10, 12-14, 16-17, 19, 21, 23-25, 28-32, 34-41, and 43 were amended; claims 1, 20, and 33 were canceled. Claims 2-19, 21-32, and 34-43 are pending.

Reasons for Allowance

2. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) a logic verification system having a set of simulation systems using remote procedure calls to connect with a diagnostic system that is connected to a set of tests (Dearth et al, U.S. Patent 5,732,247);

(2) a method of simulation with RTL and HDL models using sockets in the UNIX operating system (Stapleton, U.S. Patent 6,167,363); and

(3) a method of using a wrapper program to connect the Ptolemy design environment to an instruction set simulator (Liu et al, "Software Timing Analysis Using HW/SW Cosimulation and Instruction Set Simulator").

2.1 Applicants' first set of claims consists of claims 2-16.

Independent claim 6 is directed to a logic verification system. This claim identifies the distinct combination of features of: "a verification kernel, wherein the verification kernel

includes a diagnostic kernel and a simulation kernel, wherein the diagnostic kernel and the simulation kernel communicate through the interprocess communication mechanism" and "wherein the logic design, the logic design wrapper and the simulation kernel are linked to form a logic simulator".

Because the closest prior art does not appear to teach or suggest the combination of a diagnostic kernel and a simulation kernel communicating through an interprocess communication mechanism and a logic simulator formed by linking together a logic design, logic design wrapper and simulation kernel, claims 2-16 are deemed allowable.

2.2 Applicants' second set of claims consists of claims 17-18.

Independent claim 17 is directed to a logic verification system. This claim identifies the distinct combination of features of: "a verification environment, wherein the verification environment includes two or more layers of abstraction placed between logic being verified and a diagnostic program, wherein one of the layers of abstraction is a verification kernel, wherein the verification kernel includes a diagnostic kernel and a simulation kernel and wherein the diagnostic kernel and the simulation kernel communicate through the interprocess communication mechanism" and "wherein the verification environment further includes a plurality of ports, including an event port, wherein the event port drives and captures events".

Because the closest prior art does not appear to teach or suggest the combination of a diagnostic kernel and a simulation kernel communicating through an interprocess

communication mechanism and a verification environment having an event port that drives and captures events, claims 17-18 are deemed allowable.

2.3 Applicants' third set of claims consists of claim 19.

Independent claim 19 is directed to a logic verification system. This claim identifies the distinct combination of features of: "a verification environment, wherein the verification environment includes two or more layers of abstraction placed between logic being verified and a diagnostic program, wherein one of the layers of abstraction is a verification kernel, wherein the verification kernel includes a diagnostic kernel and a simulation kernel and wherein the diagnostic kernel and the simulation kernel communicate through the interprocess communication mechanism" and "wherein the verification environment diagnostic program generates stimulus via a DPI apply".

Because the closest prior art does not appear to teach or suggest the combination of a diagnostic kernel and a simulation kernel communicating through an interprocess communication mechanism and a verification environment diagnostic program generating a stimulus via a DPI apply, claim 19 is deemed allowable.

2.4 Applicants' fourth set of claims consists of claims 21-22.

Independent claim 21 is directed to a method of verifying an electronic system. This claim identifies the distinct combination of features of: "defining a wrapper, wherein the wrapper is an interface between the logic design and the verification kernel" and "wherein defining a wrapper includes compiling the logic design and the wrapper into an object file,

wherein the object file is linked with verification kernel routines to create an executable logic simulator".

Because the closest prior art does not appear to teach or suggest the creation of an executable logic simulator using a wrapper complied with the logic design and linked with verification kernel routines, claims 21-22 are deemed allowable.

2.5 Applicants' fifth set of claims consists of claims 23-29.

Independent claim 24 is directed to a method of verifying an electronic system. This claim identifies the distinct combination of features of: "defining a wrapper, wherein the wrapper is an interface between the logic design and the verification kernel," "executing the tests against the logic design," and "wherein executing includes executing recovery code when an exception is detected."

Because the closest prior art does not appear to teach or suggest the execution of recovery code when an exception is detected while executing tests against a logic design using a wrapper, the wrapper being an interface between the logic design a verification kernel, claims 23-29 are deemed allowable.

2.6 Applicants' sixth set of claims consists of claims 30 and 32.

Independent claim 30 is directed to a method of verifying an electronic system. This claim identifies the distinct combination of features of: "defining a wrapper, wherein the wrapper is an interface between the logic design and the verification kernel," "executing the tests

against the logic design," and "wherein executing includes popping wiggles off a wiggle queue and popping bundles off one or more bundles queues."

Because the closest prior art does not appear to teach or suggest the popping of wiggles off a wiggles queue and bundles off one or more bundles queues while executing tests against a logic design using a wrapper, the wrapper being an interface between the logic design a verification kernel, claims 30 and 32 are deemed allowable.

2.7 Applicants' seventh set of claims consists of claim 31.

Independent claim 31 is directed to a method of verifying an electronic system. This claim identifies the distinct combination of features of: "defining a wrapper, wherein the wrapper is an interface between the logic design and the verification kernel," "executing the tests against the logic design," and "wherein executing includes referencing memories built using memory access PLI tasks."

Because the closest prior art does not appear to teach or suggest the referencing of memories built using memory access PLI tasks while executing tests against a logic design using a wrapper, the wrapper being an interface between the logic design a verification kernel, claim 31 is deemed allowable.

2.8 Applicants' eighth set of claims consists of claims 34-40.

Independent claim 34 is directed to a system for simulating operation of an electronic device. This claim identifies the distinct combination of features of: "an interprocess communication mechanism for transferring stimulus from the diagnostic system to the hardware

simulator and for transferring results from the hardware simulator to the diagnostic system" and "wherein the hardware simulator includes a simulator kernel, logic design wrapper and a logic design representative of the electronic device."

Because the closest prior art does not appear to teach or suggest the combination of an interprocess communication mechanism transferring data from a hardware simulator and a diagnostic system, with the hardware simulator including a simulator kernel, logic design wrapper, and logic design, claims 34-40 are deemed allowable.

2.9 Applicants' ninth set of claims consists of claims 41-42.

Independent claim 41 is directed to a system for simulating operation of an electronic device. This claim identifies the distinct combination of features of: "an interprocess communication mechanism for transferring stimulus from the diagnostic system to the hardware simulator and for transferring results from the hardware simulator to the diagnostic system" and "wherein the diagnostic system includes a plurality of ports, including an event port, wherein the event port drives and captures events."

Because the closest prior art does not appear to teach or suggest the combination of an interprocess communication mechanism transferring data from a hardware simulator and a diagnostic system, with the diagnostic system including an event port that drives and captures events, claims 41-42 are deemed allowable.

2.10 Applicants' tenth set of claims consists of claim 43.

Independent claim 43 is directed to a system for simulating operation of an electronic device. This claim identifies the distinct combination of features of: "an interprocess communication mechanism for transferring stimulus from the diagnostic system to the hardware simulator and for transferring results from the hardware simulator to the diagnostic system" and "wherein the diagnostic program generates stimulus via a DPI apply."

Because the closest prior art does not appear to teach or suggest the combination of an interprocess communication mechanism transferring data from a hardware simulator and a diagnostic system, with the diagnostic system running a diagnostic program that generates stimulus via a DPI apply, claims 43 is deemed allowable.

3. Any comments considered necessary by Applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose current telephone number is (703) 305-1026. This telephone number will be changed to (571) 272-3709 effective 1 October 2004. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, currently can be reached at (703) 305-9704. This telephone number

will be changed to (571) 272-3716 effective 1 October 2004. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER